Metal Hard-Mask Based Double Patterning for 22nm and Beyond

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ABSTRACT

In this paper, metal hard-mask-based patterning schemes are proposed to pattern 30/30-nm line/space structures and 40-nm contact holes at 80 nm pitch. Various litho and etch approaches are compared and discussed.

INTRODUCTION

Looking at the 2008 ITRS roadmap for Logic and DRAM for contacts and metal 1 trenches, it becomes clear that by 2011 contact holes in the order of 40 nm at a pitch of 80 nm are required, while 30-nm trenches at a pitch of 60 nm will need to be standardly patterned by 2013 [1]. To get early access to these dimensions and pitches in order to explore patterning, metallization and other process steps, state-of-the-art single-print 193-nm water-based immersion lithography cannot offer a solution, even at NA values of 1.35. Despite being a very promising technique for the future, EUV lithography needs to further improve through-put, overlay performance and resist systems [2]. In order to bridge the gap between standard 193-nm immersion litho and EUV however, double-patterning and double-exposure techniques can be used.

PATTERNING 30-NM HALF-PITCH TRENCHES

Litho considerations

Several double patterning options have been explored to generate narrow-pitch trenches, such as LELE (litho-etch-litho-etch), LPLE (litho-process-litho-etch) and SDDP (spacer-defined double patterning). In this paper, the focus is on 30-nm half-pitch trenches, patterned with a LELE route, where the design is split over two lithography steps [3]. First, 60-nm trenches are printed at a pitch of 120 nm, which are subsequently shrunk down to 30 nm, using a plasma-assisted polymer deposition technique [4]. After etching trenches in a hard-mask (HM) and ashing the resist, this sequence is repeated, resulting in 30/30 nm trenches in the HM, which are finally etched into the underlying dielectric (Fig. 1). It is obvious that this patterning scheme puts stringent requirements on overlay performance and CD uniformity after the litho steps. As the final CD variation for the 30-nm wide trenches should be less than 10% 3σ after etch (i.e. less than 3 nm 3σ), these strict specifications were already applied to the original 60 nm trenches after litho. Typical 3σ values that were achieved amounted to 2.5 nm after litho and 2.6 nm after the full patterning.
Etch and stack considerations

The etch steps clearly define the final CD and pitch. The shrink process in particular, is very important for the quality of the final result. As the plasma-assisted shrink process was observed to introduce additional proximity effects [4], the shrink process and the subsequent hard-mask opening need to be taken into account when optical proximity corrections are performed. Also, the hard-mask needs to be carefully selected: first of all, it should enable double patterning. This means it should withstand the ashing chemistry used to strip the BARC and resist after the first and second hard-mask openings, and it should be thin enough not to cause too much topography for the second litho step. Secondly, it should offer sufficient etch selectivity to the underlying dielectric layer, minimizing HM faceting, HM corner-rounding, linewidth roughness and CD gain as much as possible. Thirdly, its deposition process should be compatible with the nature of the underlying dielectric, which is likely to be a low-k material with \( k < 3.0 \) for the technology nodes where 30-nm half-pitch trenches will be used. An additional interesting feature of the masking material could be its limited transparency, which could decouple the litho performance from the nature of the underlying dielectric. It would be equally interesting if it was fully sacrificial, and would be removed in e.g. the CMP step after metalization. Metallic hard-masks (MHH) (e.g. TiN) fit these requirements very well, and even offer additional advantages: they allow shifting the resist strip step from the end of the patterning sequence to before the dielectric etch step. In this way, the low-k sidewalls are not exposed during the strip step, which limits plasma damage to the low-k. Etch and strip damage is widely recognized as one of the key challenges for the integration of advanced low-k materials [5][6].
Fig. 2. Examples of potential MFM-related issues: grass formation (top left), profile control (top right), line-wigging (bottom left) and TiF residue formation (bottom right).

However, next to all the MFM advantages, several disadvantages of the use of MFM have been observed as well (Fig. 2). Grass formation during low-k etch for instance, was found to be linked to the presence of Ti-containing residues on the surface of the low-k material to be etched [7]. Profile control issues may be linked to the redeposition of non-volatile Ti-containing residues on the sidewalls, giving rise to sloped trenches and etch-stop phenomena. This issue can be mediated by increasing the substrate temperature [8]. Alternatively, plasma damage may weaken the low-k material at the sidewalls, causing the damaged layer to be removed during wet clean, when dilute HF is used for instance. This leads to undercut under the MFM. Line-wigging is typically attributed to the release of residual stress in the HM during etch [9], which results in undulating, bending or even collapsing low-k lines. Fig. 3 shows that the thickness of the MFM and the aspect ratio of the low-k lines both play a role in determining the extent of wigging. Finally, plasma damage to the dielectric may weaken the structure, which increases the risk of wigging. Tweaking the properties of the MFM to reduce its stress level without sacrificing too much selectivity to the low-k was found to be the most appropriate way of dealing with line-wigging. Moreover, the risk of wigging for a given structure can be modeled [9]; the model input parameters are basic properties of all the layers in the stack (e.g. elastic modulus, thermal expansion coefficient and residual stress) and the lay-out of the structure. The output parameter – the ‘buckling coefficient’ – predicts how high the risk of wigging is. Residue growth on the MFM after low-k etch has often been observed: it is mostly attributed to the formation of TiF outgrowths [10]. Their formation should be carefully avoided as these residues hamper metalization of the trenches. Etch chamber condition issues may arise from sputtering metallic species onto the chamber parts during low-k etch. Appropriate chamber clean, chamber conditioning and chamber monitoring procedures need to be put into place in order to avoid chamber-related issues.

Plasma damage to the low-k dielectric is probably the most important patterning issue to consider for the technology nodes where 90/90 nm trenches will be used for the metal 1 level. As
stated above, using a MHM-patterning scheme helps to minimize the damage inflicted by the ashing step. This was proven to be true for materials with $k = 3.0$ [6], where the sidewall damage depth could be reduced from 25 nm to 5 nm by switching from a resist-based patterning approach to a MHM-based scheme. However, for $k = 2.5$ materials, the use of a metal hard-mask in itself did not appear to be sufficient [11]; after MHM-opening and strip, EF-TEM carbon intensity maps indicated that carbon depletion extended in an isotropic way underneath the MHM for a large number of strip chemistries. The nature of the ashing plasma was found to be important: as can be seen from Fig. 4, even for 90/90 nm L/S trenches the impact of different strips on time-dependent dielectric breakdown (TDBB) results varies significantly, when all other processing steps are kept constant. For narrower trenches, the effect of plasma damage along the sidewalls will be even more outspoken, as a higher percentage of the low-$k$ material will be damaged than for 90-nm half-pitch lines. Simulations taking into account moisture absorption in 5 nm of damaged material on each side of the line indicated that for a $k = 2.5$ material, it would be more beneficial to use oxide than low-$k$ for 20/20 nm L/S structures. Probably the simplest way to avoid strip damage altogether would be to introduce a second HM layer underneath the MHM. It should be impenetrable to the ashing plasma, compatible with the underlying low-$k$ dielectric and (partially) removable by CMP. That low-$k$ materials can be integrated successfully in 30-nm half-pitch metal 1 structures, is proven in Fig. 5, where excellent yield for a low $k = 3.0$ low-$k$ is obtained for 1-em meander-fork structures [12].
Fig. 4: TDDB results for 90/90 nm meander-forks at 100°C, with measurement points for both O2/C12- and O2/C2H4-ashed wafers and extrapolation to 0.11 MV/cm [11] (E-model was used because it gives the most conservative lifetime prediction at low fields).

Fig. 5: Electrical yield for 30/30 nm 1-cm meander-forks (continuity and leakage)

**Alternative for metal hard-mask**

As an alternative for MHM, organic masks have been proposed [13]; these masks appear to show far fewer problems with line-wiggling because the stress in the mask layers is either low or easily controllable. Obviously, none of the specific MHM-related issues that were discussed above, would be present when organic masks are used. On the other hand, stripping these organic
layers would have to be done after the full trench etch, which would increase the plasma budget the trench sidewalls would be subjected to. Even more cumbersome would be the fact that double patterning would become very difficult with an organic mask: after the Si-containing layer on top of the organic mask layer would have been opened using the first litho photo, the resist and the BARC would have to be ashed while the carbon mask layer is exposed (Fig. 6). This would be difficult with many strip chemistries. However, it was observed that when a He/H₂ chemistry is used in a downstream plasma ash chamber at elevated temperature, ash selectivities of over 150:1 can be reached between 193-nm immersion resist and an amorphous carbon layer deposited at 400 °C. This easily allows resist and BARC ash while the carbon layer is exposed. Moreover, the same plasma conditions were proven to inflict no plasma damage to low-k materials with a k down to 2.3 [14]. This would allow stripping the carbon layer (very long strip times would be needed but this chemistry does strip) without damaging the low-k material. All in all, this strip chemistry could enable low-damage low-k patterning using a carbon mask for double patterning of 20-nm half-pitch structures.

Fig. 6: Stack with carbon mask before and after Si-mask opening (for litho photo A), showing exposed carbon layer material when the resist and BARC need to be stripped.

PATTERNING 40-NM HALF-PITCH CONTACT HOLES

Litho considerations

To generate 40-nm half-pitch contact holes (CH) problems such as limited litho resolution by the low aerial image contrast associated with dark field masks, and the 2-D character of CH as a limiting factor in the use of extreme resolution enhancement techniques, need to be overcome. One way of doing this, is by deconvoluting the 2-D CH into two exposures of lines (essentially 1-D structures). Lines with widths in the order of 40 nm can be printed at a pitch of 80 nm by making use of dipole exposures [15]. When a second exposure is added at an offset angle of 90 degrees, and both positive tone resist and positive tone development are used, the result after development would be dots of 40 by 40 nm. There are several ways to convert these dots into contact holes. Most of them involve complicated and numerous intermediate
steps, such as spinning and patterning additional coatings, mask-freezing, etc. Negative tone development, however, was found to constitute a simple method to go straight from exposure to development and end up with holes of the right size and pitch in the resist mask.

Alternatively, EUV lithography offers a straightforward way of obtaining 40-nm half pitch contacts after litho only. However, as stated before, this technique needs optimizations in several areas before it will be ready for production.

**Mask considerations**

As we move along the ITRS roadmap towards the most advanced technology nodes, the resist thickness for contact hole patterning appears to decrease to values below 100 nm, while the aspect ratio of the contact holes has seen a dramatic increase from less than 3:1 for the 0.35 μm node to over 5:1 for the 22 nm node. The combination of these trends makes clear that an additional mask is needed to pattern the contacts for the most advanced technologies. Both MHM (TaN) and organic masks have been evaluated for contact holes. Selectivities of over 150:1 can be obtained for TaN, but sufficiently good selectivity for carbon masks has been reported as well [16]. The use of TaN does however imply the same etch chamber contamination risk as for the patterning of 30-nm half-pitch trenches (see above). Both TaN and carbon masks were tested on double-exposed wafers and on EUV-litho wafers, and both types of hard-masks were found to yield excellent results. Fig. 7 shows successfully patterned 80-nm pitch contact holes after EUV litho on a carbon mask, while Fig. 8 displays top-down images for 40 nm contacts at a similar pitch after double exposure litho and after TaN HM patterning.

![Image of 80-nm pitch contacts](image1.png)

**CONCLUSIONS**

For 30-nm half-pitch trenches and 40-nm half-pitch contacts, patterning routes were proposed and discussed, taking into account various litho, etch and stack approaches and
considerations. It was proven that for both types of structures, satisfactory results can be obtained after careful litho, etch and stack optimization.

ACKNOWLEDGMENTS

The Imec BEOL litho and integration teams are gratefully acknowledged for valuable input.

REFERENCES

1. ITRS roadmap 2008